CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a plurality of CAM cells;

match lines coupled to respective rows of the CAM cells;

storage circuits coupled to the match lines and configured to store, in response to assertion of a first timing signal, match indications signaled on the match lines; and

a timing control circuit coupled to the storage circuits and configured to assert the first timing signal at either a first instant or a second instant according to the state of a mode select signal.

2. The CAM device of claim 1 wherein the timing control circuit receives a clock signal and a first compare signal, and wherein the second instant occurs at least one cycle of the clock signal after the first compare signal is asserted.

3. The CAM device of claim 2 wherein the first instant occurs prior to the second instant and after the compare signal is asserted.

4. The CAM device of claim 2 wherein the second instant is substantially coincident with a selected transition of the clock signal that occurs at least one cycle of the clock signal after the first compare signal is asserted.

5. The CAM device of claim 4 wherein the selected transition of the clock signal follows a first transition of the clock signal, the first transition of the clock signal occurring after the first compare signal is asserted.

6. The CAM device of claim 5 wherein the first transition of the clock signal and the selected transition of the clock signal are both rising edge transitions of the clock signal.

7. The CAM device of claim 5 wherein the first instant occurs after the first transition of the clock signal and prior to the selected transition of the clock signal.

8. The CAM device of claim 7 wherein the timing control circuit comprises a delay circuit to enable assertion of the first timing signal after a delay interval following the first transition of the clock signal, the length of the delay interval determining the first instant.

9. The CAM device of claim 8 wherein the delay circuit includes a select input to receive a delay control value, the delay circuit being responsive to the delay control value to select one of a plurality of different time intervals to be the delay interval.

10. The CAM device of claim 9 further comprising a configuration circuit to store a value indicative of the delay control value.

11. The CAM device of claim 10 wherein the configuration circuit comprises a run-time programmable configuration register.

12. The CAM device of claim 10 wherein the configuration circuit comprises a storage location to store a value that controls the state of the mode select signal.

13. The CAM device of claim 1 further comprising an integrated circuit contact to receive a signal that controls the state of the mode select signal.

14. The CAM device of claim 1 wherein the second instant coincides with an edge of a clock signal.

15. The CAM device of claim 1 wherein the timing control circuit comprises a delay circuit to enable assertion of the first timing signal after a delay interval, the length of the delay interval determining the first instant.

16. The CAM device of claim 15 wherein the delay circuit comprises a select circuit to select one of a plurality of different time intervals to be the delay interval according to the state of a delay control value.

17. The CAM device of claim 15 further comprising a one-shot circuit coupled to an output of the delay circuit and configured to assert the timing control signal for a period of time after the delay interval.

18. The CAM device of claim 1 wherein the timing control circuit comprises:
a first timing circuit to assert a first intermediate timing signal at the first instant;
a second timing circuit to assert a second intermediate timing signal at the second instant; and
a select circuit to select, in response to the mode select signal, either the first intermediate timing signal or the second intermediate timing signal to be the first timing signal.

19. The CAM device of claim 18 wherein the second timing circuit is configured to assert the second intermediate timing signal at a time substantially coincident with a selected transition of a clock signal.

20. The CAM device of claim 19 wherein the first timing circuit is configured to assert the first intermediate timing signal a delay time after a first transition of the clock signal, the first transition of the clock signal preceding the selected transition of the clock signal, and the delay time being less than the time interval between the first transition of the clock signal and the selected transition of the clock signal.

21. A content addressable memory (CAM) device comprising:

a CAM array to generate a plurality of match indications;

a configuration circuit to store a delay control value;

a timing control circuit coupled to receive the delay control value from the configuration circuit and configured to generate a timing control signal a delay time after assertion of a first control signal, the delay time being selected from one of a plurality of different time intervals according to the delay control value; and

a storage circuit coupled to receive the match indications from the CAM array and configured to store match indications in response to the timing control signal.

22. The CAM device of claim 21 wherein the configuration circuit is a run-time programmable storage register.

23. The CAM device of claim 22 wherein the configuration circuit comprises fused elements that are blown in a programming operation to store the delay control value.

24. A method of operation within a content addressable memory (CAM) device comprising:

generating a plurality of match indications in response to assertion of a compare signal; and

storing the plurality of match indications at either a first time or a second time according to

the state of a mode select signal.

25. The method of claim 24 wherein generating a plurality of match indications in response to assertion of a compare signal comprises asserting a compare enable signal in response to a transition of a clock signal that occurs after assertion of the compare signal, the compare enable signal enabling a comparand value to be output to an array of CAM cells within the CAM device for comparison with contents thereof.

26. The method of claim 24 wherein storing the plurality of match indications at the second time comprises storing the plurality of match indications substantially coincidentally with a selected clock signal transition that follows assertion of the compare signal.

27. The method of claim 26 wherein storing the plurality of match indications substantially coincidentally with a selected clock signal transition:

detecting a first transition of the clock signal that follows assertion of the compare signal;

detecting a second transition of the clock signal that follows the first transition of the clock signal; and

storing the plurality of match indications in response to the second transition of the clock signal.

28. The method of claim 27 wherein the first transition of the clock signal and the second transition of the clock signal are both rising edge transitions of the clock signal.

29. The method of claim 27 wherein storing the match indications at the second time comprises storing the plurality of match indications after the first transition of the clock signal and prior to the second transition of the clock signal.

30. The method of claim 24 wherein storing the match indications at the second time comprises delaying for a first time interval after assertion of the compare signal before storing the match indications.

31. The method of claim 30 wherein delaying for a first time interval comprises delaying for a time required for a timing signal to propagate through a delay circuit.

32. The method of claim 31 further comprising outputting a delay control value to the delay circuit to select one of a plurality of different times required for the timing signal propagate through the delay circuit.

33. The method of claim 32 further comprising storing the delay control value within a configuration circuit of the CAM device.

34. The method of claim 33 wherein storing the delay control value within the configuration circuit comprises issuing an instruction to a control circuit of the CAM device, the instruction instructing the control circuit to store the delay control value within the configuration circuit.

35. The method of claim 33 wherein storing the delay control value within a configuration circuit of the CAM device comprises programming the delay control value within the configuration circuit in a one-time programming operation.

36. The method of claim 35 wherein programming the delay control value within the configuration circuit in a one-time programming operation comprises blowing one or more

fused elements within the CAM device.

37. The method of claim 24 wherein generating the plurality of match indications comprises generating signal levels on a plurality of match lines of the CAM device, and wherein storing the plurality of match indications at either a first time or a second time comprises asserting a detect signal at either the first time or the second time to enable a plurality of logic circuits to generate logic level outputs according to respective signal levels on the plurality of match lines.

38. The method of claim 37 wherein generating signal levels on a plurality of match lines of the CAM device comprises selectively discharging the match lines of the CAM device according to whether corresponding data words stored within the CAM device match a comparand value.

39. The method of claim 24 wherein storing the plurality of match indications at either a first time or a second time comprises generating a pulse at either the first time or the second time to enable a plurality of storage circuits to store the match indications.

40. The method of claim 24 wherein generating a pulse at either the first time or the second time to enable a plurality of storage circuits to store the match indications comprises asserting and then deasserting a latch enable signal to enable a plurality of latch circuits to store the match indications.

41. The method of claim 24 further comprising generating a match address that corresponds to a selected one of the match indications.

42. The method of claim 24 further comprising setting the mode select signal to a first state during a wafer test of the CAM device and setting the mode select signal to a second state during normal operation of the CAM device.

43. The method of claim 42 wherein setting the mode select signal to the first state comprises contacting a contact point of the CAM device with a test probe.

44. A content addressable memory (CAM) device comprising:
means for generating a plurality of match indications in response to assertion of a compare signal; and
means for storing the plurality of match indications at either a first time or a second, later time according to the state of a mode select signal.

45. The CAM device of claim 44 wherein the means for storing the match indications at the second time comprises means for storing the plurality of match indications after a first transition of a clock signal and prior to a second transition of the clock signal.

46. The CAM device of claim 45 wherein the means for storing the match indications at the first time comprises means for storing the plurality of match indications in response to the second transition of the clock signal.